

Shuo REN

Email: sren@cse.cuhk.edu.hk · renshuo139@gmail.com · shuoren-mike.github.io

PhD researcher building long-horizon, tool-grounded LLM agents for complex engineering workflows. Research spans multi-agent physical-design optimization, failure-conditioned repair, and automatically generated evaluation environments, grounded in verifiable EDA and mathematical-optimization tools.



Internship & Education

Research Intern, EDA Research Lab, Hong Kong Science Park

May 2026–Present

Developing agentic 3D-IC workflows that couple LLM agents with industrial physical-design tools and feedback for partitioning and design-space exploration.

Research Collaboration, ABCO Project (CUHK Industry Collaboration)

Mar 2025–Apr 2026

Built the physical-design-to-architecture feedback loop behind [CLIP-3D](#), connecting analytical 3D floorplanning with gem5, McPAT, CACTI, and HotSpot.

The Chinese University of Hong Kong (CUHK)

Sep 2024–Present

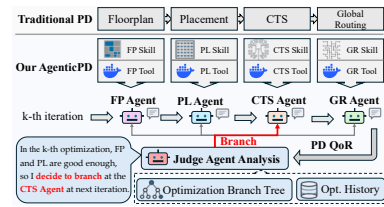
PhD in CSE, full postgraduate studentship; working with Prof. Tsung-Yi Ho and Prof. Bei Yu

Huazhong University of Science and Technology (HUST)

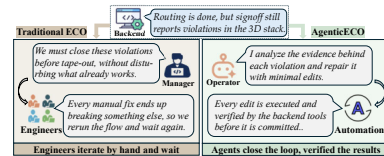
2020–2024

BEng in Computer Science and Technology; GPA 3.93/4.00, top 1.5%; National Scholarship of China

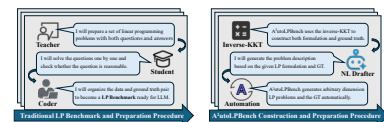
Selected Agent Research



AgenticPD (ASP-DAC 2027) [\[paper\]](#) [\[code\]](#) built a multi-agent chip physical-design optimizer that **outperformed AutoTuner and ORFS-Agent on post-route WNS across all six design/technology pairs** at the same 20-evaluation budget. Designed stage-aware search, tool interfaces, and reusable design states; won 7/9 comparisons against a single agent across DeepSeek, Qwen, and Kimi backbones.



AgenticECO [\[paper\]](#) [\[code\]](#) built an automated 3D-IC chip repair system combining diagnosis, parallel candidate search, and minimal-disturbance routing. **Cleared DRC in 7/9 cases versus 2/9 for stock repair and full reroute** under matched budgets; changed only 0.66% of nets on average in cleared cases, touching no clocks. A cross-backbone rerun cleared all nine cases, with seven passing all checks and 0.44% mean net disturbance.



A²utoLPBench [\[paper\]](#) [\[code\]](#) built an end-to-end agent evaluation platform with automatic task generation, known-optimum verification, Docker execution, and trajectory/token-cost auditing. An inverse-KKT generator supplies difficulty-controlled tasks without manual answer labeling. Evaluated six model families; the solver-critic loop **raised Kimi-K2.5's solve rate from 15.1% to 30.2%** on a 53-item MAMO Complex subset.

EDA Research Background

Partitioning-Free 3D-IC Floorplanning (ASP-DAC 2026) [\[paper\]](#), jointly optimized chip block placement and die assignment, achieving shorter wirelength than six baselines on all five GSRC benchmarks.

CLIP-3D [\[paper\]](#), connected chip architecture and physical evaluation; improved realized BIPS by 13.75% on average (up to 24.77%) over shelf-pack across 48 thermally binding configurations. Featured as a 3D-IC case study in an IDAS 2026 keynote.

Chiplet3D [\[paper\]](#), co-optimized chiplet pin placement and 3D thermal fields, reducing wirelength by 39–43% on average and peak temperature by up to 45.9°C versus baselines; validated temperatures with 3D-ICE.

Technical Stack

Agent/LLM: Python; tool-use and multi-agent systems; structured tool APIs; Docker evaluation harnesses; trajectory, failure, and token-cost analysis; AI-native development with Claude Code and Codex.

EDA/Systems: C/C++, Linux, Git; OpenROAD/ORFS and Innovus; physical design, STA, and 3D-IC workflows; gem5, McPAT, CACTI, and HotSpot.